

Symbolic Model Checking with Partitioned Transition Relations

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October 1991

CMU-CS-91-195

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Winner of the Sidney Michaelson Best Paper Award at VLSI 91,
Edinburgh, Scotland.

This research was sponsored in part by the Avionics Laboratory, Wright Research and Development Center, Aeronautical Systems Division (AFSC), U.S. Air Force, Wright-Patterson AFB, Ohio 45433-6543 under Contract F33615-90-C-1465, ARPA Order No. 7597 and in part by the National Science Foundation under Contract No. CCR-9005992.

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Keywords: Logic design verification, Binary decision diagrams, Partitioned transition relations, Asynchronous circuits, Breadth first search

Abstract

We significantly reduce the complexity of BDD-based symbolic verification by using *partitioned transition relations* to represent state transition graphs. This method can be applied to both synchronous and asynchronous circuits. The times necessary to verify a synchronous pipeline and an asynchronous stack are both bounded by a low polynomial in the size of the circuit. We were able to handle stacks with over 10^{50} reachable states and pipelines with over 10^{120} reachable states.

1 Introduction

Although methods for verifying sequential circuits by searching their state transition graphs have been investigated for many years, it is only recently that such methods have begun to seem practical. Before, the largest circuits that could be verified had about 10^6 states. Now it is easy to check circuits that have many orders of magnitude more states [3, 5, 6, 7]. The reason for the dramatic increase is the use of special data structures such as binary decision diagrams (BDDs) [2] for encoding the state transition graphs of such systems.

In this paper, we show how to process state transition graphs more efficiently than in our previous work [5, 6]. Our new approach involves using multiple BDDs, which are implicitly conjuncted or disjuncted, to represent the graphs. We call this kind of representation a *partitioned transition relation*. The BDDs that make up the partitioned transition relation are derived in a natural way from the structure of the circuit being verified. We illustrate the power of the technique by verifying an asynchronous stack [10] and a synchronous pipeline circuit [5]. Using a partitioned transition relation, we were able to verify a stack 32 bits wide and 2 cells deep. For comparison, we were unable to verify a stack only 1 bit wide and 1 cell deep when using a single BDD to represent the transition relation because the transition relation required more than 350,000 BDD nodes. For a pipeline with 4 registers, each 32 bits wide, the partitioned transition relation required less than 2,500 BDD nodes, while using a single BDD required nearly 340,000 nodes, a savings of nearly a factor of 140. On a Sun 4, the verification time improved from approximately 14,000 seconds (projected) to 995 seconds, a factor of about 14. We were also able to handle example pipelines with over 10^{120} reachable states.

There are several other methods that use BDDs in the verification of sequential circuits. Bryant and Seger [3] use a symbolic switch-level simulator to check pre- and post-conditions specified in a restricted form of temporal logic. The logic allows boolean conjunction and the next time modality (**X**). Coudert, Berthet, and Madre describe a system for showing equivalence between deterministic finite automata [7]. Their system performs a symbolic breadth-first search of the state space reachable by the product of the two automata. None of these methods can easily handle nondeterministic systems. With transition relations, it is very natural to model examples like

the cache coherency protocol for the Encore Gigamax, which McMillan has recently investigated [11]. A major feature of the Gigamax architecture is an asynchronous, and hence nondeterministic, interconnection network. The use of abstraction to hide certain details of the cache replacement policy also gives rise to nondeterminism in this example.

2 Symbolic verification

Given a circuit, let V be its set of boolean state variables. We identify a boolean formula over V with the set of valuations which make the formula true. A valuation of the variables corresponds in a natural way to a state of the circuit; hence the formula may be thought of as representing a set of circuit states. The BDD for the formula is in practice a concise representation for this set of states. In the remainder of the paper, we will denote sets of states using S and T . We denote the BDD representing the set S by $S(V)$, where V is the set of variables that the BDD depends on. In addition to representing sets of states of a circuit, we must represent the transitions that the circuit can make. To do this, we use a second set of variables V' . A valuation for the variables in V and V' can be viewed as designating a pair of states in the circuit, and we can represent sets of pairs using BDDs as above. We will refer to sets of pairs of states as transition relations. If N is a transition relation, then we write $N(V, V')$ to denote the BDD that represents it.

There are many finite state verification methods that can make effective use of this representation [5, 7]. For our purposes, the important property of these algorithms is that the basic step is performing computations of the following form:

$$S'(V') = \bigvee_{v \in V} [S(V) \wedge N(V, V')].$$

(The notation above indicates a series of nested existential quantifications, one for each variable in V .) This expression, called a relational product, gives the set of states S' reachable in one step from the set of states S in a circuit with transition relation N . It is crucial to be able to do this computation efficiently. A special algorithm is typically used to do this operation in one pass over the BDDs $S(V)$ and $N(V, V')$. By using such an algorithm, it is possible to avoid building the BDD for $S(V) \wedge N(V, V')$, which would often

be impractically large. Unfortunately, the BDD $N(V, V')$ itself is often very big. Up to this point, being forced to construct this BDD has been the major stumbling block in trying to verify complex circuits. In the following sections, we describe how to overcome this problem by using a partitioned transition relation to represent N .

3 Deriving transition relations

The first step in verifying a circuit is to derive its transition relation. Our goal is to reflect the structure of the circuit in the structure of the transition relation, so that the transition relation can be stored and manipulated more efficiently.

For a synchronous circuit with n state variables, we let $V = \{v_0, \dots, v_{n-1}\}$ and $V' = \{v'_0, \dots, v'_{n-1}\}$. For each state variable v_i , there is a piece of combinational logic which determines how it is updated. Let f_i be the function computed by this logic. Then the value of v_i in the next state is given by

$$v'_i = f_i(V).$$

These equations are used to define the relations

$$N_i(V, V') = (v'_i \Leftrightarrow f_i(V)).$$

In a legal transition of the circuit, each N_i must be true; hence the transition relation for the circuit is

$$N(V, V') = N_0(V, V') \wedge \dots \wedge N_{n-1}(V, V').$$

Thus, the transition relation for a synchronous circuit can be expressed as a conjunction of relations.

In practice, each N_i can often be represented by a small BDD (typically fewer than 100 nodes). However, the size of the BDD representing the entire transition relation may grow as the product of the sizes of the individual parts, and thus may be prohibitively large. In the past, this has been the major limitation of symbolic model checking. For our new method, we instead represent the transition relation by a list of the parts, which are implicitly conjuncted. We call this representation a conjunctive partitioned transition relation.

Asynchronous circuits can be modeled with a conjunctive partitioned transition relation, like synchronous circuits, and can also be represented by a disjunctive partitioned transition relation. To simplify the description of how these forms of transition relation are computed, we assume that all the components of the circuit have exactly one output, and have no internal state variables. It is straightforward to generalize the method to handle cases where this assumption does not hold.

In asynchronous circuits, there can be an arbitrary delay between when a transition is enabled and when it actually occurs. We can model this by allowing each component to nondeterministically choose whether to transition its output, resulting in a conjunctive partitioned relation with n parts, all of the form

$$N_i(V, V') = (v'_i \Leftrightarrow f_i(V)) \vee (v'_i \Leftrightarrow v_i).$$

For some components, such as C-elements and flip-flops, the function $f_i(V)$ may depend on the current value of the output of the component, as well as the inputs.

The above model for asynchronous circuits allows wires to transition concurrently. We can also use an interleaving model, which allows only one wire to transition at a time. This idea can be used to construct a disjunctive partitioned transition relation, as follows. First, apply distributivity to the conjunction of the R_i , giving a disjunction of 2^n terms. Each of these terms corresponds to the simultaneous transition of some subset of the n wires in the circuit. Second, keep only those terms that correspond to exactly one wire transitioning. This results in a disjunction of the form

$$N(V, V') = N_0(V, V') \vee \cdots \vee N_{n-1}(V, V')$$

where

$$N_i(V, V') = (v'_i \Leftrightarrow f_i(V)) \wedge \bigwedge_{j \neq i} (v'_j \Leftrightarrow v_j).$$

We represent the full transition relation as a list of the $N_i(V, V')$, which are implicitly disjuncted.

4 Computing relational products

As noted earlier, computing relational products is a fundamental operation in many symbolic verification methods. This section describes how relational

products can be computed using the representations described in the previous section. These techniques significantly increase the size of circuits that can be verified compared to previous methods.

For a disjunctive partitioned transition relation, the relational product computed is of the form

$$S'(V') = \bigvee_{v \in V} [S(V) \wedge (N_0(V, V') \vee \cdots \vee N_{n-1}(V, V'))].$$

This relational product can be computed without ever constructing the BDD for the full transition relation by rewriting $S'(V')$.

$$S'(V') = \bigvee_{v \in V} [S(V) \wedge N_0(V, V')] \vee \cdots \vee \bigvee_{v \in V} [S(V) \wedge N_{n-1}(V, V')].$$

Thus, we are able to reduce the problem of computing $S'(V')$ to one of computing a series of relational products involving relatively small BDDs. This technique was used previously for verifying asynchronous circuits [5]. Much larger asynchronous circuits could be verified using this method than with a monolithic transition relation.

For a conjunctive partitioned transition relation, the relational product computed is of the form

$$S'(V') = \bigvee_{v \in V} [S(V) \wedge (N_0(V, V') \wedge \cdots \wedge N_{n-1}(V, V'))]. \quad (1)$$

The main difficulty in computing $S'(V')$ without building the conjunction is that conjunction does not distribute over existential quantification. The method given below overcomes this difficulty.

Our new technique is based on two observations. First, circuits exhibit locality, so many of the $N_i(V, V')$ will depend on only a small number of the variables in V and V' . Second, although conjunction does not distribute over existential quantification, subformulas can be moved out of the scope of existential quantification if they do not depend on any of the variables being quantified. We will take advantage of these observations by conjuncting the $N_i(V, V')$ with $S(V)$ one at a time and quantifying out each variable v when none of the remaining $N_i(V, V')$ depend on v . More formally, the user must choose a permutation ρ of $\{0, \dots, n-1\}$. This permutation determines the

order in which the $N_i(V, V')$ are conjuncted. For each i , let D_i be the set of variables in V that $N_i(V, V')$ depends on. Also, let

$$E_i = D_{\rho(i)} - \bigcup_{k=i+1}^{n-1} D_{\rho(k)}.$$

Thus, E_i is the set of variables contained in $D_{\rho(i)}$ that are not contained in $D_{\rho(k)}$ for any k larger than i . The E_i are pairwise disjoint and their union is equal to V . The relational product in equation 1 can be computed as

$$\begin{aligned} S_1(V, V') &= \bigvee_{v \in E_0} [S(V) \wedge N_{\rho(0)}(V, V')] \\ S_2(V, V') &= \bigvee_{v \in E_1} [S_1(V, V') \wedge N_{\rho(1)}(V, V')] \\ &\vdots \\ S'(V') &= \bigvee_{v \in E_{n-1}} [S_{n-1}(V, V') \wedge N_{\rho(n-1)}(V, V')]. \end{aligned}$$

The ordering ρ has a significant impact on how early in the computation state variables can be quantified out. This affects the size of the BDDs constructed and the efficiency of the verification procedure. Thus, it is important to choose ρ carefully, just as with the BDD variable ordering. In practice, we have found it fairly easy to come up with orderings which give good results.

In the previous section, we described how a circuit could be represented by a set of $N_i(V, V')$, each depending on exactly one variable in V' . While this is almost always more efficient than constructing the full transition relation, it may not be the best choice. As long as the BDDs do not get too large, it is better to combine several of the $N_i(V, V')$ into one BDD by forming their disjunction or conjunction.

5 Verifying asynchronous circuits

Asynchronous circuits can be verified in two steps. First, compute the set of states the circuit, composed with an environment, can reach from a given set of initial states. Then check that no hazard can occur in any of the reachable states. Finding the reachable states is the most computationally

expensive of these two steps. In practice, checking for hazards is usually done as the reachable states are computed. This is similar to Dill's [9] method for verifying safety properties of asynchronous circuits.

The set of reachable states is found by computing the least fixed point S of

$$S(V') = S_0(V') \vee \bigvee_{v \in V} [S(V) \wedge N(V, V')],$$

where S_0 is the initial set of states and N is the transition relation of the circuit. We use frontier set simplification to speed up the computation of this fixed point [5, 7]

There are significant differences in the complexity of doing reachability analysis using conjunctive and disjunctive partitioned transition relations. Consider two uncoupled systems M' and M'' with disjoint sets of state variables V' and V'' . Let M be the composition of these two systems. This is an unrealistic example, but it helps illustrate what happens when computing the reachable states of loosely coupled systems. The BDD $S(V)$ representing the set of reachable states of M is equal to $S'(V') \wedge S''(V'')$, where $S'(V')$ ($S''(V'')$) is the BDD for the reachable states of M' (M''), and $V = V' \cup V''$. An efficient way to order the BDD variables of the combined system in this case is to have all the variables of one component (say M') before any of the variables in the other component. Then the number of BDD nodes in $S(V)$ is equal to the sum of the nodes in $S'(V')$ and $S''(V'')$, independent of whether conjunctive or disjunctive partitioning is used. However, the sizes of the BDDs representing the intermediate state sets are potentially different for the two methods.

Let $S_i(V)$, $S'_i(V')$ and $S''_i(V'')$ be the BDDs representing the states reachable in i steps by M , M' and M'' , respectively, using non-interleaved semantics. Similarly, let $T_i(V)$, $T'_i(V')$ and $T''_i(V'')$ be the BDDs representing the states reachable in i steps by M , M' and M'' , respectively, using interleaved semantics. In the conjunctive case, $S_i(V) = S'_i(V') \wedge S''_i(V'')$, so the size of each $S_i(V)$ is equal to the sum of the sizes of $S'_i(V')$ and $S''_i(V'')$, just as for the set of reachable states. However, for the disjunctive case,

$$T_i(V) = \bigvee_{k=0}^i T'_k(V') \wedge T''_{i-k}(V'').$$

Thus, interleaving semantics introduces an artificial correlation between the local states of M' and M'' in the $T_i(V)$. The $T_i(V)$ are generally much larger

