CURRICULUM VITAE

Edmund M. Clarke

TITLE: FORE Systems University Professor of Computer Science and
Professor of Electrical and Computer Engineering

OFFICE: Carnegie Mellon University
Department of Computer Science
5000 Forbes Avenue
Pittsburgh, PA 15213
412-268-2628

Address: 457 Old Farm Road
Pittsburgh, PA   15228
412-571-0794

Citizenship: USA

Marital Status: Married, three sons, four grandchildren

EDUCATION:

Cornell University, Ithaca, NY: Doctor of Philosophy, Computer Science, September 1976; Master of Science, Computer Science, August 1974.

Duke University, Durham, NC: Master of Arts, Mathematics, August 1968.

University of Virginia, Charlottesville, VA: Bachelor of Arts with High Distinction, Mathematics, June 1967.

HONORS, AWARDS, FELLOWSHIPS and PATENTS AWARDED:

Einstein Professorship – Chinese Academy of Sciences, 2013

Honorary Doctorate – Vienna University of Technology, 2012

American Academy of Arts and Sciences - Clarke is among 212 other leaders in the sciences, social sciences, the humanities, the arts, business and public affairs to be elected as a member of this prestigious institution.

CADE Herbrand Award for **Distinguished Contributions to Automated Reasoning** in recognition of his role in the invention of Model Checking and his sustained leadership in the area for more than two decades, 2008.

ACM Turing Award for role in developing **Model Checking** into a highly effective verification technology widely adopted in the hardware and software industries, shared with E. Allen Emerson and Joseph Sifakis, 2007.

National Academy of Engineering for contributions to the formal verification of hardware and software correctness, 2005.

Fellow of the Institute of Electrical and Electronics Engineers (IEEE), 2005.

IEEE Harry H. Goode Memorial Award for significant and pioneering contributions to formal verification of hardware and software systems, and for the profound impact these contributions have had on the electronics industry, 2004.

Allen Newell Award for Research Excellence, Carnegie Mellon University, Department of Computer Science, 1999.

ACM Paris Kanellakis Theory and Practice Award for the development of symbolic **Model Checking** with Randy Bryant, Allen Emerson and Kenneth McMillan, 1998.

Fellow of the Association for Computing Machinery (ACM), 1998.

Semiconductor Research Corporation Technical Excellence Award, 1995.

The Sidney Michaelson Best Paper Award, VLSI'91.

Cornell University: NDEA Fellowship (1 year), IBM Research Fellowship (2 years).

Duke University: Woodrow Wilson Fellowship, Sigma Xi.

University of Virginia: Phi Beta Kappa, Echols Scholar, Intermediate Honors, Phi Eta Sigma, University Scholar, Graduated with High Distinction.

U.S. PATENT
TITLE: METHOD AND SYSTEM TO VERIFY A CIRCUIT DESIGN BY VERIFYING CONSISTENCY BETWEEN TWO DIFFERENT LANGUAGE REPESENTAIONS OF A CIRCUIT DESIGN, Patent # 7,225,417 B2, Date of patent: May, 29, 2007, Inventors: Edmund M. Clarke, Daniel Kroening, and Karen Yorav.

PH.D. THESIS:

Ph.D. Degree: Cornell University, awarded September 1, 1976.

Thesis Title: Completeness and Incompleteness Theorems for Hoare-like Axiom Systems.

Thesis Advisor: Professor Robert Constable.

ACADEMIC POSITIONS:

Carnegie Mellon University, Pittsburgh, PA: University Professor, 2008-present.

Carnegie Mellon University, Pittsburgh, PA: courtesy appointment in the Electrical and Computer Engineering Department, May 1996 – 2008.

Carnegie Mellon University, Pittsburgh, PA: FORE Systems Professor of Computer Science, April 1995-present.

Carnegie Mellon University, Pittsburgh, PA: Professor, School of Computer Science, September l990-April 1995.

Carnegie Mellon University, Pittsburgh, PA: Associate Professor, School of Computer Science, September l982-September 1990. Received Tenure in 1986.

Harvard University, Cambridge, MA: Assistant Professor, Division of Applied Sciences, September 1978-August l982.

Duke University, Durham, NC: Assistant Professor, Computer Science Department, September 1976-August 1978.

Cornell University, Ithaca, NY: Research Assistant and Graduate Student, Computer Science Department, September 1972-August 1976.

Madison College, Harrisonburg, VA: Assistant Professor, Department of Mathematics, September 1968-August 1972.

RESEARCH INTERESTS:

Model Checking

Software and hardware verification

Automatic theorem proving and symbolic computation

Implementation of symbolic algorithms on parallel machines

Hardware description languages

Concurrent and distributed programming languages

Semantics programming languages

Theory of computation

STUDENTS RECEIVING PH.D. DEGREE:

Sicun Gao, Computable Analysis, Decision Procedures, and Hybrid Automata: A New Framework for the Formal Verification of Cyber-Physical Systems, 2012

Himanshu Jain, Verification Using Satisfiability Checking, Predicate Abstraction, and Craig Interpolation, 2008

Nishant Sinha, Automated Compositional Analysis for Checking Component Substitutability, December, 2007.

Pankaj Kumar Chauhan, Verification of Large Industrial Circuits Using SAT Based Reparameterization and Automated Abstraction-Refinement, May, 2007.

Muralidhar Talupur, Abstraction Techniques for Parameterized Verification, July, 2006.

Anubhav Gupta, Learning Abstractions for Model Checking, June 2006.

Sagar Chaki, A Counterexample Guided Abstraction Refinement Framework for Verifying Concurrent C Programs, May, 2005.

Alex Groce, Error Explanation and Fault Localization with Distance Metrics, March, 2005.

S. Berezin, Model Checking and Theorem Proving: A Unified Framework, April, 2002; Current Position: Postdoc, Stanford University, Stanford, CA.

W. Marrero, BRUTUS: A Model Checker for Security Protocols, June, 2001; Current Position: Assistant Professor, DePaul University, Chicago, IL.

Y. Lu, Automatic Abstraction for Model Checking, May 2000; Current Position: Broadcom, San Jose, CA.

M. Minea, Model Checking with Partial Order Reduction for Real-Time Systems, December 1999; Current Position: Postdoctoral Researcher in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley.

V. Hartonas-Garmhausen, Probabilistic Symbolic Model Checking with Engineering Models and Applications, Engineering and Public Policy, Carnegie Mellon University, April, 1998.

S. Jha, Symmetry and Induction in Model Checking, October 1996; Current Position: Assistant Professor, University of Wisconsin, Madison, WI.

S. Campos, A Quantitative Approach to the Formal Verification of Real-Time Systems, September 1996; Current Position: Associate Professor at the Computer Science Department of the Universidade Federal de Minas Gerais, city of Belo Horizonte, Brasil.

X. Zhao, Verification of Arithmetic Circuits, August 1996; Current Position: Intel Corporation, Beaverton, OR.

D.E. Long, Model Checking, Abstraction and Modular Verification, August 1993; Current Position: AT&T Bell Laboratories, Murray Hill, NJ.

J.R. Burch, Trace Algebra for Automatic Verification of Real-Time Concurrent Systems, August 1992; First Position: Post-Doctoral Research, Department of Computer Science, Stanford University; Current Position: Cadence Berkeley Laboratories.

K.L. McMillan, Symbolic Model Checking, May 1992; First Position: AT&T Bell Laboratories, Murray Hill, NJ. (McMillan's thesis was a co-winner of the 1992 ACM Doctoral Dissertation Award); Current Position: Cadence Berkeley Laboratories.

M.C. Browne, Automatic Verification of Sequential Circuits, Carnegie Mellon University, January 1989; First Position: Project Scientist on Warp and Nectar projects, Carnegie Mellon University; Current Position: Sun Computer Corporation, CA.

D.L. Dill, Automatic Verification of Asynchronous Circuits using Automata, Carnegie Mellon University, August 1987; Current Position: Tenured Full Professor, Stanford University. (Dill's thesis tied for second place in the ACM Dissertation Award Contest and published as an ACM Distinguished Dissertation).

B. Mishra, Graph Theoretic Algorithms and the Design of VLSI Systems, Carnegie Mellon Unversity, September 1985; Current Position: Tenured Full Professor, Courant Institute of Mathematical Sciences, New York University.

A.P. Sistla, Theoretical Issues in the Design and Verification of Distributed Systems, Harvard University, July 1983; First position: Tenured Full Professor, University of Massachusetts, Amherst; Current Position: Tenured Associate Professor, University of Illinois at Chicago.

C.N. Nikolaou, Reliability Issues in Distributed Systems, Harvard University, June 1982; First Position: Manager, Multi-systems Resource Management group, IBM T.J. Watson Research Center, Yorktown Heights, New York; Current Position: University of Crete, Greece.

E.A. Emerson, Branching Time Temporal Logic and the Design of Correct Concurrent Programs, Harvard University, August 1981; Current Position: Tenured Full Professor, University of Texas, Austin.

STUDENTS RECEIVING M.S. DEGREE:

Anneliese K. von Mayrhauser, Proving Parallel Programs Correct, Duke University, July 1978. Currently Assistant vice President for Research Colorado State University.

Bruce W. Ballard, Systematic Removal of Recursion for a Class of Lisp-like Recursion Schemes, Duke University, May 1977.

PH.D.THESIS COMMITTEES:

Shuvendu Lahiri, Advisor: Randy Bryant, Computer Science Department, Carnegie Mellon University, 2004.

Sanjit Seshia, Advisor: Randy Bryant, Computer Science Department, Carnegie Mellon University, 2005.

A.L. Turk, Advisor: Gary J. Powers, Chemical Engineering Department, Carnegie Mellon University.

M. Velev, Advisor: Randy Bryant, Computer Science Department, Carnegie Mellon University.

A. Chutinan, Advisor: Bruce Krogh, Electrical and Computer Engineering Department, Carnegie Mellon University.

Y.-A. Chen, Advisor: Randy Bryant, Computer Science Department, Carnegie Mellon University.

K. Stirewalt, Advisor: Gregory Abowd, Department of Computer Science, Georgia Institute of Technology.

A. Jain, Advisor: Randy Bryant, Electrical and Computer Engineering Department, Carnegie Mellon University.

J. Dingel, Advisor: Steve Brookes, Computer Science Department, Carnegie Mellon University.

S. Older, Advisor: Steve Brookes, Computer Science Department, Carnegie Mellon University.

M. Kaltenbach, Advisor: J. Mishra, Computer Science Department, University of Texas, Austin, 1996.

S. Probst, Advisor: Gary Powers, Chemical Engineering, Carnegie Mellon University.

A. Gupta, Advisor: Allan Fisher, Computer Science Department, Carnegie Mellon University.

D. Beatty, Advisor: Randy Bryant, Computer Science Department, Carnegie Mellon University.

I. Moon, Automatic Verification of Discrete Chemical Process Control Systems, August 1992; Advisor: Gary Powers, Chemical Engineering, Carnegie Mellon University.

O. Coudert, SIAM: A Toolbox for the Formal Proof of Sequential Systems, L'Ecole National Superieure Des Telecommunications, Paris, France, October 1991.

M. Petkovsek, Finding Closed-Form Solutions of Difference Equations by Symbolic Methods, September 1990; Advisor: Dana Scott, Computer Science Department, Carnegie Mellon University.

CURRENT PH.D GRADUATE STUDENTS

William Klieber
Anvesh Komuravelli
Soon Ho Kong
Samir Sapra
Qinsi Wang
Cory Bevilaqua

CURRENT POST-DOCTORAL STUDENTS AND VISITORS

Liu Bing	2012 - continuing
Sicun Gao	2012 - continuing
Fuyuan Zhang	2012 - 2013

FORMER GRADUATE STUDENTS, POST DOCS, AND VISITING SCIENTISTS

Post - Docs

Haijun Gong	2009 - 2012
Michael Wang	2012
Paolo Zuliani	2008-2012
Silke Wagner	2008 - 2009
Axel Legay	2008-2009
Kwang Kuen Yi	2008
Lei Bu	2007 - 2008
Alexandre Donze	2007 - 2008
Azadeh Farzan	2007 - 2008

James Kapinski	2007
Constantinos Bartzis	2004-2007
Tamir Heyman	2005-2007
Haifeng Zhu	2005-2006
Alaexandar Nanevski	2005
Prasanna Thati	2005
Daniel Milam	2005
Prasanna Thati	2004
Ansgar Fehnker	2003-2004
Micheal Theobald	2001-2004
Joel Ouaknine	2002-2004
Tayssir Touili	2003-2004
Daniel Kroening	2001-2004
Karen Yorav	2002-2003
Ofer Strichman	2001-2003
K. Schmidt	2000-2001
Helmut Veith	1999-2000
Armin Biere	1997-1998
W. Heinle	1997-1998
S. Shankar	1997-1998
Y. Zhu	1997-1998
D. Deharbe	1995-1997

Visitors

Orna Grumberg	2011, 2012
Qiusong Yang	2011, 2012
Fuyan Zhang	2012
Marius Minea	2012, 2013
Daniel Kroenig	2012
Qinxiang Cao	2012
Zhengwei Qi	2011
Fei He	2010
Kwang Keun Yi	2008
Lei Bu	2007
Ingo Feinerer	2007
I. Feinerer	2007
B. Wang	
A. Platzer	2007
Y. Chen	2007
W. Windsteiger	2005-2006
Y. Tsay	
X. Li	
F. Tiplea	
Marcos Oliveira	2001

F. Wang   2001
G.H. Kwon   1999-2000, 2007
P. Williams   1999-2000
S. Shanker   1997
S. Krischner   1993
T. Filkorn   1992
H. Hiraishi   1988, 1994
H. Hamaguchi   1993
P. Granger   1992
H. Schlingloff   1991
J. P. Vidal   1990
O. Grumberg   1985-1987, Summers 1988-2007
T. Yoneda   1990
S. Kimura   1989
T. Tang   1986
Y. Q. Sun   1986
Y. Feng   1985

COURSES TAUGHT AT CMU, HARVARD, AND DUKE:

Special Topics in Software Systems: Practical Design Decisions, spring 2007.

Bug Catching: Automated Program Verification and Testing, CMU, fall 2007.

Fast SAT Solvers and Practical Decision Procedures, CMU, spring 2006.

Bug Catching: Automated Program Verification and Testing, CMU, fall 2006.

Specification, Verification and Model Checking, CMU, spring 2005.

Compiler Design, CMU, fall 2005.

Formal Languages and Automata: CMU, Spring 2002.

Bug-Catching: Automated Program Verification and Testing: CMU, fall 2001.

Mathematical Foundations of Computer Science: CMU, fall 1999, spring 2001.

Program Analysis and Abstract Interpretation: CMU, fall 2000.

Verification of Concurrent, Real-time, and Reactive Systems: CMU, six times, most recently, spring 2000.

Formal Languages, Automata, and Computability Theory (Elementary FLAC): CMU, fall 1997.

Advanced Programming in Mathematica (for Students in the Sciences and Engineering): CMU, spring 1997.

Theory of Algorithms: CMU, three times, most recently during the spring of 1995.

Formal Languages and Automata Theory: three times, most recently at CMU during the fall of 1991.

Comparative Programming Languages: Duke, spring 1977; Harvard, fall 1978; CMU fall 1986, spring 1988, spring 1989.

Hardware Verification (with Randy Bryant, Allan Fisher, and Carl Seger): CMU, fall 1989.

Term Rewriting Systems (with J. Wing): CMU, spring 1989.
Topics in Automatic Theorem Proving: CMU, fall 1988.

Theory of Logic Programming: CMU, spring 1987.

Fundamental Structures of Programming: CMU, fall 1984-1985.

Programming Language Issues in VLSI Design: CMU, spring 1985.

Compiler Design: seven times, most recently at CMU during the spring of 1984.

Logics of Programs and Program Verification: Harvard, spring 1980-82; CMU, spring 1984.

Programming Language Semantics: Duke, fall 1976; Harvard, spring 1979.

Elementary Programming: Duke, spring 1977-1978.

Software Engineering: Duke, fall 1977.

EDITORIAL BOARDS, PANELS AND COMMITTEES:

Former Editor-In-Chief:

FORMAL METHODS IN SYSTEM DESIGN, Kluwer Academic Publishers.

Editorial Boards:

IEEE TRANSACTIONS ON SOFTWARE ENGINEERING, published by IEEE Computer Society.

MICROELECTRONICS JOURNAL, published by Elsevier.

JOURNAL OF SOFTWARE (CHINESE), published by Science Press.

DISTRIBUTED COMPUTING, published by Springer Verlag, 1986-2000.

LOGIC AND COMPUTATION, published by Oxford University Press, 1990-93.

ACM TRANSACTIONS ON DESIGN AUTOMATION OF ELECTRONIC SYSTEMS (TODAES), published by the ACM, 1996-99.

Advisory Board:

SOFTWARE TOOLS AND TECHNOLOGY TRANSFER, published by Springer Verlag.

Panels and Committees:

Accellera (unification of **Open Verilog International** and **VHDL International**) committee to design a specification language for verification and simulation, 1998-2000.

Workshop Organizer: Software Model Checking, Carnegie Mellon University, Pittsburgh, Pennsylvania, March 24, 2003.

External Review Committee, Computer Science Department of Indiana University. Bloomington, Indiana, October 20-22, 2002.

Program Committee, Correct Hardware Design and Verification Methods (CHARME), Livingston, Scotland, UK, September 2001.

Steering Committee (Program Committee), CAV'01, Conference on Computer-Aided Verification, Paris, France, July 18-22, 2001.

NSF Review Panel for Science and Technology Centers, Arlington, Virginia, Nov 16-17, 2000.

Program Committee, FMCAD '00, Third International Conference on Formal Methods in Computer Aided Design, Austin, Texas, November , 2000.

Scientific Advisory Board, ISIS '00, Information Systems for Industrial Control and Supervision, Linköping, Sweden, 1998-present.

Program Committee, FM'99, The World Congress on Formal Methods in Computing Systems Development, Toulouse, France, October, 1999.

Steering Committee (Program Committee), CAV'99, Conference on Computer-Aided Verification, Trento, Italy, July 7-10, 1999.

Steering Committee, ARTS'99, 5th International AMAST Workshop on Real-Time and Probabilistic Systems, Bomberg, Germany, May 26-28, 1999.

Steering Committee, (FloC '99) The 1999 Federated Logic Conference, Formal Methods and Security Protocol, Tento, Italy, July 5, 1999.

Program Committee, CONCUR'98, Nice, France, September 8-11, 1998.

Program Committee, CSD'98, International Conference on Applications of Concurrency to System Design, Fukushima, Japan, March 23-26, 1998.

Program Committee, CHARME '97, IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, Montreal, Quebec, Canada, October 16-18, 1997.

Program Committee, 9th International Conference on Computer Aided Verification, Haifa, Israel, June 1997.

Program Committee, CHDL '97: The IFIP Conference on Hardware Description Languages and their Applications.

ACM Workshop on Strategic Directions in Computing Research, Co-Chair (with J. Wing) of Formal Methods Working Group, June 14-15, 1996.

Program Chairman, 11th Annual IEEE Symposium on Logic in Computer Science, New Brunswick, NJ, July, 1996.

Program Committee, FMCAD '96: International Conference on Formal Methods in Computer-Aided Design, Palo Alto, CA, November 1996.

Steering Committee, DIMACS Year of Logic, 1996.

Program Committee, Computer-Aided Verification, CAV'95, 1995.

Program Committee, CHDL'95: The IFIP Conference on Hardware Description Languages and their Applications.

Program Committee, Reed-Muller'95: IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansion in Circuit Design, 1995.

NSF/NIST Workshop on Integrated Policy Making, George Mason University, Fairfax, VA, December, 13-15, 1995.

Program Committee, CHARME'95, IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, 1995.

Program Committee, Logic in Computer Science, 1995.

Program Committee, ICALP, 1995.

Steering Committee, Logic in Computer Science, 1994-present.

Program Committee, Logic in Computer Science, 1994.

Program Committee, ICALP, 1994.

Program Committee, First International Conference on Temporal Logic, 1994.

Program Committee: 1993 Conference on Computer-Aided Verification (CAV), Heraklion, Crete, Greece, June 28 - July 1, 1993.

NSF Panel on Young Investigator Awards, Washington, DC, April 14-16, 1993.

NSF Panel on Institutional Infrastructure Program, November 30 - December 1, 1993.

Program Committee, CHDL '93: The IFIP Conference on Hardware Description Languages and their Applications, IMEC, Leuven, Belgium, October 9, 1992.

Organizing Committee: 1992 Conference on Logic in Computer Science (LICS), Toronto, Canada, June 1992.

Program Committee, International Conference on Theorem Provers in Circuit Design, Nijmegen, The Netherlands, June 22-24, 1992.

Program Committee, 1992 Conference on Automated Deduction (CADE11), Saratoga Springs, NY, June 15-18, 1992.

Program Committee, Workshop on Computer-Aided Verification (CAV'91), Aalborg University, Denmark, July 1-4, 1991.

Program Committee, 1991 International Symposium on Computer Hardware Description Languages (CHDL 91), Marseille, France, April 22-24, 1991.

NSF Panel on Institutional Infrastructure Small Scale Proposals in Computer and Information Science and Engineering, Washington, DC, September 17, 1990.

Program Committee, Workshop on Computer-Aided Verification (CAV'90), New Brunswick, NJ, June 1990.

Program Committee, 1990 Conference on Logic in Computer Science (LICS), University of Pennsylvania, Philadelphia, PA, June 1990.

Panel on Joint NSF/DARPA Initiative in Formal Methods, Washington, D.C., May 3, 1990.

NSF panel on Research Initiation Awards in Software Systems, March and April, 1990.

Steering Committee (with Robert Kurshan, Joseph Sifakis and Amir Pnueli), Conference on Computer-Aided Verification, 1990-present.

Program Committee, IFIP international Workshop on Applied Formal Methods for Correct VLSI Design, Leuven, Belgium, November 13-16, 1989.

Program Committee, 1989 ACM Symposium on Principles of Distributed Computing, Edmonton, Canada, August 14-16, 1989.

Program Committee, 1989 International Symposium on Computer Hardware Description Languages, Washington, DC, June 19-21, 1989.

Organizer (with Joseph Sifakis and Amir Pnueli), Workshop on Automatic Verification Methods for Finite State Systems, Grenoble, France, June 12-14, 1989.

Program Committee, 1989 International Conference on Computing and Information, Toronto, Canada, May 1989.

Program Committee and Session Chairman, 1989 IEEE Computer Society Workshop on VLSI, Clearwater Beach, FL, February 19-22, 1989.

Program Committee, Interdisciplinary Conference on Axiomatic Systems, Columbus, OH, December 15-18, 1988.

Midterm site visit committee to University Indianna for NSF CER program, September 1988.

Program Committee of Fourteenth Annual ACM Symposium on Principles of Programming Languages.

Program Committee of 8th International Conference on Computer Hardware Description Languages.

Member of IFIP WG 10.5 on Computer Hardware Description Languages.

Initial site visit committee to Indiana University for NSF CER program, October 1985.

Program Committee for Logics of Programs, 1985.

NASA Formal Verification/Design Proof Peer Review for the SIFT Flight Control System, Georgia Institute of Technology, Atlanta, GA, July 7-8, 1983.

Organizer (with Dexter Kozen) of Logics of Programs 1983, Pittsburgh, PA, June 1983.

Program Committee and Session Chairman for 11th Annual ACM Symposium on Principles of Programming Languages.

Program Committee and Session Chairman for 3rd Annual ACM Symposium on Principles of Distributed Systems.

Program Committee and Session Chairman 22nd IEEE Symposium on Foundations of Computer Science, October 28-30, 1981.

Local arrangements (with Steve Schuman of Massachusetts Computer Associates) for meeting of International Federation for Information Processing Working Group 2.4 on System Implementation Languages, Harvard Faculty Club, December 4-6, 1980.

PROFESSIONAL ORGANIZATIONS:

IFIP WG 10.5 on Hardware Description Languages, ACM, IEEE, European Association for Theoretical Computer Science.

REFEREE:

NSF grants and many technical journals including JACM, CACM, ACM TOPLAS, IEEE-TSE, Acta Informatica, SIAM Journal of Computing, Theoretical Computer Science, Information Processing Letters.

CONSULTING POSITIONS:

Nextop, Mumbai, India

NEC Princeton Labs, Princeton, NJ.

Synopsys, Inc. Beaverton, OR, 2000- 2002.

BOPS (Billions of Operations Per Second, Inc.), Technical Advisory Board, Mt. View, CA, 2000-2001.

Verysys Design Automation, Chief Scientist for Model Checking, Inc., Fremont, CA, 1999.

Intel Design Development Systems, Intel Corporation, Hillsboro, OR, March 20-24, 1995.

Cadence Corporation, San Jose, CA, June 10, 1994.

Intel Supercomputing Systems Division, Intel Corporation, Beaverton, OR, May 17-20, 1993.

Intel Design Development Division, Intel Corporation, Haifa, Israel, May 11, 1992.

Fujitsu America, Inc., San Jose, CA, January 1, 1991-Present.

Encore Computer Corporation, 257 Cedar Hill Street, October 18, 1990, Verification of Cache Coherency Protocol for Gigamax Multiprocessor.

AT&T Bell Laboratories, Murray Hill, NJ, June 2-6, 1986. I worked with R. P. Kurshan on techniques for automatically verifying finite state concurrent systems.

Masssachusetts Computer Associates, Inc., 26 Princess Street, Wakefield, MA, Summers 1980 and 1981. I worked with Steve Schuman on distributed implementations of the multitasking features in ADA.

Bolt, Beranek and Newman, Cambridge, MA, Consultant on Defense Communications Agency Contract DCA100-78-C-0028, Summer 1979. My work was concerned with the evaluation of the multiprocessing features in the ADA programming language and resulted in the production (with Arthur Evans, Robert Morgan and Eric Roberts) of a technical report entitled "The Impact of Multiprocessor Technology on High-Level Language Design".

LECTURES AT PROFESSIONAL MEETINGS AND OTHER UNIVERSITIES:

Major Invited Lectures:

Einstein Professorship, Beijing, PRC, October 2013

Heidelberg Laureates 2013, Frankfurt, Germany, September 2013

SAT 2013, Keynote Address, Helsinki, Finland, July 2013

TSD 2013, Keynote Address, Beijing, China, April 2013

Elba Island, Italy, 2011

Lipari

Lugano Summer School, Lugano, Switzerland, July, 2007.

Seoul National University, Korean lecture series; Samsung Inc., Electronics and Telecommunications Research Institute, Kyonggi University, June, 2007.

iCAST - International Collaboration for Advanced Security Technology Conference, Taipei, Taiwan, May, 2007.

Triangle Distinguished Lecture, UNC, Chapel Hill, Raleigh-Durham, NC, Jan, 2007.

General Motors Research Workshop, Bangalore, India, Jan, 2007.

Japanese Society for the Promotion of Science (JSPS) – Tsukuba University, , University of Tokyo, Kyto Sangyo University, Osaka University, AIST-CVS, Japan, October, 2006.

VMCAI Conference, Charleston, SC, Oct, 2006.

Isaac Newton Institute, Constraints and Verification Workshop, Cambridge, UK, May, 2006.

UIUC Distinguished Lecture Series, University of Illinois at Urbana-Champaign, IL, April, 2006.

Distinguished Lecture Series, Stony Brook University, New York, Nov, 2005.

Leadership in Research and Education Conference, Department of Computer Science, 40th Anniversary celebration, Cornell University, Ithaca, NY, October, 2005.

International School for Computer Science Researchers, Lipari, Italy, July 2005.

NATO-VISSAS Advanced Research Workshop, Romania, March, 2005.

Verification Grand Challenge Workshop, Menlo Park, CA, Feb, 2005.

IBM Verification Seminar, Haifa, Israel, Nov-2004.

SAT-based Counterexample Guided Abstraction Refinement in Model Checking, CADE-19 Miami, Florida, July 28-August 2, 2003.

TIME-ICTL Conference, Cairns, Australia July 8-10, 2003.

Formal Techniques for Networked and Distributed Systems (FORTE 2002), Rice University, Houston , Texas, November 11-14, 2002.

Eighth International Conference on Principles and practice of Constraint Programming (CP2002). Cornell University, Ithaca, New York, September 8-13, 2002.

SAT-based Counterexample Guided Abstraction Refinement in Temporal Logic Model Checking, Symposium on Theory and Applications of Satisfiability Testing (SAT 2002), Cincinnati, Ohio, May 6-9 2002.

SAT-based Counterexample Guided Abstraction Refinement, European Joint Conference on Theory and Practice of Software (ETAPS-SPIN 2002), Grenoble, France, April 9-13 2002.

Grand Challenge: Model Checking Software Vienna University of Technology, Computer Science Department, Institute of Information Systems, Vienna, Austria, April 8 2002.

City University Graduate Center in New York, NY, March 13-15, 2002.

Grand Challenge: Model Checking Software, University of Illinois at Chicago, Chicago, Illinois, March 2-7 2002.

Model Checking Without BDDs, Intel Formal Verification Symposium, Haifa, Israel, July 24, 2001.

State of the Art in Model Checking, Invited Lecturer, Design for Safety 2000 Workshop, Moffett Training & Conference Center, NASA Ames Research Center, October 11, 2000.

Progress on the State Explosion Problem in Model Checking, Invited Speaker, Informatics - 10 Years Back, 10 Years Ahead, Dagstuhl Tenth Anniversary Celebration, International Conference and Research Center for Computer Science, Schloss Dagstuhl, August 27-31 2000.

Symbolic Model Checking with and without BDDs, Distinguished Lecture, University of California at Santa Barbara, May 8, 2000.

Symbolic Model Checking with and without BDDs, Distinguished Lecture, Michigan State University, April 19-20, 2000.

Symbolic Model Checking without BDDs, Invited Lecture, Mathematical Foundations of Programming Semantics (MFPS XVI), Stevens Institute of Technology, April 13-16, 2000.

Counterexample Driven Abstraction Refinement, Invited Speaker, Model Checking and Program Analysis, Schloss Ringberg, Germany, February 20-23, 2000.

Model Checking, J. Barkley Rosser Memorial Lecturer, University of Wisconsin, Madison, Wisconsin, April 21, 1999.

Model Checking, Invited Speaker, 18th Conference of the Brazilian Computer Science Society, Belo Horizonte, Brazil, August 3-7, 1998.

Model Checking, Invited Speaker, WOLLIC, 5th Workshop on Logic, Language, Information, and Computation, Sao Paulo, Brazil, July 28-31, 1998.

Model Checking: A Historical Perspective, TABLEAUX'98, International Conference on Analytic Tableaux and Related Methods, Oisterwijk, The Netherlands, May 5-8, 1998.

Model Checking Perspective, 21st Century Engineering Consortium, Melbourne, FL, March 17-19, 1998.

Model Checking Distinguished Lecture, University of Virginia, Charlottesville, VA, January 26, 1998.

Model Checking, FST&TCS'97, foundations of Software Technology and Theoretical Computer Science, Kharagpur, India, December 18-20, 1998.

Security Protocol Verification, Distinguished Lecture, University of Houston, Houston, TX, November 18, 1997.

Model Checking, Distinguished Lecture, Rice University, Houston, TX, November 17, 1997.

Temporal Logic Model Checking, ILPS'97, International Logic Programming Symposium, Port Jefferson, L.I., NY, October 12-17, 1997.

Using Compositionality for Efficient Model Checking, COMPOS'97, International Symposium on Compositionality, Malente, Germany, September 7-12, 1997.

Model Checking: Past, Present, and Future, The Intel DSTC Symposium on Formal Verification of VLSI Designs, Haifa, Israel, June 26, 1997.

Model Checking, Keynote address, The Eighth Israeli Conference on Computer Systems and Software Engineering, Herzliya, June 18, 1997.

Tutorial, ASP-DAC'97, Asian Pacific Design Automation Conference, Chiba, Japan, January 1997.

Dealing with Complexity in Temporal Logic Model Checking, CAD Techniques for Design Correctness (Specification, Modeling and Verification), Intel Corporation, Hillsboro, OR, December 1996.

Tutorial on Model-Checking, BRICS Autumn School on Verification, Aarhus, Denmark, October 28-November 1, 1996.

The 21st International Symposium on Mathematical Foundations of Computer Science, Krakow, Poland, September 2-6, 1996.

INFOSEC Research and Technology Transfer Conference, Maritime Institute of Technology and Graduate Studies, Baltimore, MD, August 6-8, 1996.

Oxford Workshop on Automated Formal Methods, Oxford University, Oxford, England, June 19-21, 1996.

DIMACS Workshop on Controllers for Manufacturing and Automation: Specfication, Synthesis, and Verification Issues, Rutgers University, NJ, May 13-15, 1996.

Workshop on Automated Deduction, Chicago, IL, April 20-21, 1996.

DIMACS Workshop on Computational and Complexity Issues in Automated Verification, Rutger University, NJ, March 25-28, 1996.

Distinguished Lecture, DIMACS Special Year on Logic and Algorithms, Rutgers University, NJ, March 22, 1996.

Distinguished Lecture, The University of Texas at Austin, Austin, TX, February 19-21, 1996.

Tutorial on Symbolic Model Checking, The Eighth International Conference on Formal Description Techniques for Distributed Systems and Communications Protocols, FORTE '95, Montreal, Quebec, Canada, October 17-20, 1995.

EURO-DAC/EURO-VHDL, Brighton, Great Britain, September 18-22, 1995.

Intel Design and Test Technology Conference, San Diego, CA, September 14, 1995.

INFOSEC Research and Technology Transfer Conference, Maritime Institute of Technology and Graduate Studies, Baltimore, MD, August 9, 1995.

Model-Checking and the Verification of Concurrent Programs, Eighth International Software Quality Week Conference, San Francisco, CA, May 30-June 2, 1995.

The Eleventh Conference on the Mathematical Foundations of Programming Semantics, New Orleans, LA, March 29-April 1, 1995.

Tutorial on Formal Hardware Verification, Intel Design Development Division, Intel Corporation, Hillsboro, Or, March 21-22, 1995.

Lecturer, NATO International Summer School, Marktoberdorf, Germany, July 26- August 7, 1994.

Logic in Computer Science, Paris, France, July 3-7, 1994.

The International Conference on Application and Theory of Petri Nets, Zaragoza, Spain, June 20-24, 1994.

The 1994 VLSI Workshop, San Diego, CA, April 27-30, 1994.

Canadian Conference on Very Large Scale Integration, Banff, Alberta, Canada, November 14-16, 1993.

Software Institute, Academica Sinica, Beijing, People's Republic of China, October 22, 1993.

REX '93: A Decade of Concurrency Reflections and Perspectives, Noordwijkerhout, The Netherlands, June 1-4, 1993.

The Johns Hopkins University, Spring 1993 IBM Distinguished Lecturer Series, April 2, 1993.

CHDL '93: The IFIP Conference on Hardware Description Languages and their Applications, Ottawa, Canada, April 26-28, 1993.

Bellcore Corporation General Research Colloquium, Bellcore Corporation, Morristown, NJ, March 19, 1993.

The 1993 VLSI Workshop, Asilomar Conference Center, Asilomar, CA, February 9-11, 1993.

Workshop on Computer-Aided Verification of Digital Circuits, sponsored by Semiconductor Systems Design Technology and Corporate Software Research and Development, Motorola, Inc., Austin, TX, October, 30, 1992.

INRS/BNR Seminar on Formal Methods Applied to Telecommunication Software, University du Quebec, Montreal, Canada, November 16, 1992.

1992 Jumelage Meeting, Cornell University, Ithaca, NY, October 15-17, 1992.

Advanced Course on Formal Verification Techniques in VLSI Design, Scuola Superiore G. Reissk Romoli, L'Aquila, Italy, July 6-10, 1992.

A Practical Introduction to Formal Hardware Verification, Tutorial at 29th ACM/IEEE Design Automation Conference and Exposition, Anaheim, CA, June 8-12, 1992.

Tutorial and Research Review on Formal Methods in Software Engineering (Concurrent and Real-Time Systems), Naval Postgraduate Center, Monterey, CA, May 20-22, 1992.

Karuizawa Workshop on Circuits and Systems, Karuizawa, Japan, April 21, 1992.

Royal Society of London, Dicussion Meeting on Mechanized Reasoning and Hardware Design, London, England, October 3-4, 1991.

SRC/MCC Workshop on Formal Verification of Hardware, Austin, TX, May 22-23, 1991.

Distinguished Lecture, SUNY Stony Brook, Stony Brook, NY, March 18, 1991.

Engineering Training and Education Seminar on Hardware Verification, Digital Equipment Corporation, Hudson, MA, November 8, 1990.

International Federation for Information Processing Working Group 2.3 Meeting, Santa Catalina Island, CA, December 10-14, 1990.

Keynote Speaker, Workshop on Computer-Aided Verification (CAV'90), New Brunswick, NJ, June 1990.

International Federation for Information Processing Working Group 2.2 Meeting, Palo Alto, CA, August 21-25, 1989.

Theory Institute on Automated Reasoning, Argonne National Laboratory, Chicago, IL, August 1-10, 1990.

Workshop on Automatic Verification Methods for Finite State Systems, Grenoble, France, June 12-14, 1989.

AAAI Spring Symposium - Representation and Compilation in High Performance Theorem Proving, Stanford University, Stanford, CA, March 28-30, 1989.

1989 IEEE VLSI Workshop, Clearwater, FL, February 16-19, 1989.

University of Maryland, Department of Computer Science, Fall '88 Colloquium Speaker, October 1988.

International Federation for Information Processing Working Group 2.3 Meeting, Pittsburgh, PA, August 15-19, 1989.

REX School/Workshop on Linear Time, Branching Time and Partial Order in Logics and Models for Concurrency, Noordwijkerhout, The Netherlands, May 30-June 3, 1988.

Shanghai Jiao Tong University, Shanghai, People's Republic of China, Series of three lectures on automatic verification of finite state concurrent systems, October 1987.

University of Science and Technology of China, Heifei, People's Republic of China, Series of three lectures on automatic verification of finite state concurrent systems, October 1987.

Institute of Mathematics, Academica Sinica, Beijing, People's Republic of China, Series of three lectures on automatic verification of finite state concurrent systems, October 1987.

Northwestern University, Xian, People's Republic of China, Series of three lectures on automatic verification of finite state concurrent systems, October 1987.

26th Annual Lake Arrowhead Conference, How Will We Specify Concurrent Systems in the Year 2000?, September 16-18, 1987.

Joint US-Japan Workshop on Logic of Programs, sponsored by NSF (US) and JSPS (Japan), Honolulu, HI, May 18-21, 1987.

Colloquium on Temporal Logic and Specification, University of Manchester, England, April 8-10, 1987.

Tutorial on Hardware Verification, University of Manchester, England, April 7, 1987.

Workshop on Formal Aspects of VLSI Design, University of Edinburgh, Scotland, July 1-5, 1985.

Summer meeting European Association for Symbolic Logic, Paris, France, July 8-12, 1985.

DARPA VLSI Contractor's Meeting, Salt Lake City, UT, March 18-20, 1985.

Workshop on Algebraic Models of Distributed Systems, Distributed Computing and Communication Lecture Series, Columbia University, New York, NY, April 26, 1985.

Workshop on Reasoning about Cooperating Agents and Concurrent Processes, sponsored by the Center for the Study of Language and Information and the American Association for Artificial Intelligence, Monterey, CA, August 22-24, 1984.

Advanced Nato Study Institute on Logics and Models for Specification and Verification of Concurrent Systems, La Colle-Sur-Loup, France, October 8-18, 1984.

Special Discussion Meeting of the Royal Society of London on Mathematical Logic and Programming Languages, London, England, February 15-16, 1984.

INVITED LECTURES:

McMasters University Hamilton, Ontario, Canada, City University Graduate Center in New York, NY, University of New South Wales Sidney, Australia, Vienna University of Technology, Computer Science Department, Institute of Information Systems, University of Illinois at Chicago, City University Graduate Center in New York, McMasters University, Michigan State (East Lansing), IBM Yorktown Heights Research Center, Duke, Carnegie-Mellon University, U. of California (Santa Barbara), MIT, Cornell, U. of Maryland, NC State, SUNY Stony Brook, Harvard, SUNY Albany, National Bureau of Standards, Xerox Palo Alto Research Center. Lawrence Livermore Laboratory, U. of Virginia, RPI, Penn State, German Mathematical Institute (Oberwolfach, West Germany), Bell Laboratories (Murray Hill, NJ), Bell Laboratories (Holmdel, NJ), Universitat des Saarlandes/Bad Honnef (West Germany), CMU NSF/SERC Seminar on Concurrency, Indiana University, Fudan University (Peoples Republic of China), University of Oldenburg (West Germany), University of Aachen (Aachen, Germany), Gesellschaft fur Mathematik und Datenverarbeitung (St. Augustin, West Germany), University of Wisconsin (Madison), University of Illinois at Chicago (Chicago, IL), Bellcore Research Laboratories

(Morristown, NJ), Fujitsu America Corporation (San Jose, CA), The Technion (Haifa, Israel), IBM (Austin, TX), The Oregon Graduate Center, Intel Supercomputer Systems Division (Beaverton, OR), Union Switch and Signal (Pittsburgh), Siemens (Munich, Germany), Technical University of Munich (Munich, Germany), New York University, National Security Agency, Advanced Micro Devices (AMD) (Austin, Tx), University of California (Berkeley), Cadence Berkeley Laboratories, McMaster University (Hamilton, Ontario, Canada), IRST (Trento, Italy), University of Michigan (Ann Arbor, MI), University of Iowa (Iowa City, IA), Saarbruecken University (Saarbruecken, Germany), Universidade do Amazonas (Brazil).

CONTRACT AND GRANT SUPPORT:

Air Force Research Laboratory
Air Force Multi University Research Initiative
Army Research Office
DARPA
Fujitsu Lab Limited
General Motors
Intel
International Collaboration for Advanced Security Technology
National Science Foundation
National Security Agency
Naval Research Laboratory
Raytheon BBN Technologies
Semiconductor Research Corporation
Siemens

SERVICE AND COMMITTEE WORK WITHIN THE UNIVERSITY:

Department of Computer Science Hiring Committee, Spring 1999.

University Committee of Investigation, Spring 1996.

University Committee on Tenure Appointments, 1991-1992.

Chairman, School of Computer Science Council, 1989-91.

Coordinator for Programming Systems, Department of Computer Science, 1985-93.

Committee on Math/CS Undergraduate Program, 1986-89.

Committee on Ph.D. program in Algorithms, Combinatorics, and Optimization, fall 1988.

Chairman of Graduate Admissions Committee, Department of Computer Science, spring 1986.

Graduate Admissions Committee, Department of Computer Science, spring 1985.

Elected to the Faculty Senate as one of the representatives from the CMU Computer Science Department, 1985-86.

Chairman, CMU Computer Science Department Qualifier Quality Review Committee.

Harvard Division of Applied Sciences Committee on Higher Degrees.

Harvard Division of Applied Sciences Undergraduate Board of Tutors in Applied Mathematics.

PUBLICATION LIST:

Papers Published in Refereed Journals:

Analysis and verification of the HMGB1 signaling pathway. Haijun Gong, Paolo Zuliani, Anvesh Komuravelli, James R. Faeder, Edmund M. Clarke: BMC Bioinformatics, 11(S-7): S10 (2010)

On simulation-based probabilistic model checking of mixed-analog circuits. Edmund M. Clarke, Alexandre Donzé, Axel Legay: Formal Methods in System Design 36(2): 97-113 (2010)

Model checking: algorithmic verification and debugging. Edmund M. Clarke, E. Allen Emerson, Joseph Sifakis: Commun. ACM 52(11): 74-84 (2009)

Functional Equivalence Verification Tools in High-Level Synthesis Flows. Anmol Mathur, Masahiro Fujita, Edmund M. Clarke, Pascal Urard: IEEE Design & Test of Computers 26(4): 88-95 (2009)

Efficient Craig interpolation for linear Diophantine (dis)equations and linear modular equations. Himanshu Jain, Edmund M. Clarke, Orna Grumberg: Formal Methods in System Design 35(1): 6-39 (2009)

Computing differential invariants of hybrid systems as fixedpoints. André Platzer, Edmund M. Clarke: Formal Methods in System Design 35(1): 98-120 (2009)

Verification of evolving software via component substitutability analysis. Sagar Chaki, Edmund M. Clarke, Natasha Sharygina, Nishant Sinha: Formal Methods in System Design 32(3): 235-266 (2008)

Word-Level Predicate-Abstraction and Refinement Techniques for Verifying RTL Verilog. Himanshu Jain, Daniel Kroening, Natasha Sharygina, Edmund M. Clarke: IEEE Trans. on CAD of Integrated Circuits and Systems 27(2): 366-379 (2008)

Verification of SpecC using predicate abstraction. Edmund M. Clarke, Himanshu Jain and Daniel Kroening:. Formal Methods in System Design 30(1): 5-28 (2007).

Checking: Software and Beyond. Edmund M. Clarke, Flavio Lerda: Model J. UCS 13(5): 639-649 (2007)

Concurrent software verification with states, events, and deadlocks. Sagar Chaki, Edmund M. Clarke, Joël Ouaknine, Natasha Sharygina, Nishant Sinha: Formal Asp. Comput. 17(4): 461-483 (2005)

An Iterative Framework for Simulation Conformance. Edmund M. Clarke, Sagar Chaki, Somesh Jha, and Helmut Veith: J. Log. Comput. 15(4): 465-488 (2005).

Computational challenges in bounded model checking. Edmund M. Clarke, Daniel Kroening, Joël Ouaknine, and Ofer Strichman: STTT 7(2): 174-183 (2005) 2004.

VeriAgent: an Approach to Integrating UML and Formal Verification Tools. Edjard Mota, Edmund M. Clarke, Alex Groce, Waleska Oliveira, Marcia Falcão, Jorge Kanda: Electr. Notes Theor. Comput. Sci. 95: 111-129 (2004)

Counterexample Guided Abstraction Refinement, Edmund M. Clarke, Orna Grumberg, Somesh Jha, Yuan Lu, and Helmut Veith, Submitted to Journal of the ACM.

Predicate Abstraction of ANSI-C Programs Using SAT Formal Methods in System Design. Edmund M. Clarke, Daniel Kroening, Natasha Sharygina and Karen Yorav: 25(2-3): 105-127 (2004)

Efficient Verification of Sequential and Concurrent C Programs Formal Methods in System Design. Edmund M. Clarke, Sagar Chaki, Alex Groce, Joël Ouaknine, Ofer Strichman, and Karen Yorav: 25(2-3): 129-166 (2004).

Modular Verification of Software Components in C. Edmund M. Clarke, Sagar Chaki, Alex Groce, Somesh Jha, and Helmut Veith: IEEE Trans. Software Eng., 30(6): 388-402 (2004)

SAT-based counterexample-guided abstraction refinement. Edmund M. Clarke, Anubhav Gupta, and Ofer Strichman: IEEE Trans. on CAD of Integrated Circuits and Systems,: 23(7): 1113-1123 (2004).

Efficient verification of security protocols using partial-order reductions. Edmund M. Clarke, Somesh Jha, and Wilfredo R. Marrero: STTT 4(2): 173-188 (2003).

Bounded Model Checking. Edmund M. Clarke, Armin Biere, Alessandro Cimatti, Ofer Strichman, and Y. Zue: Book chapter: Advances in Computers, Academic Press, 2003.

Automated Compositional Abstraction Refinement for Concurrent C Programs: A Two-Level Approach. Sagar Chaki, Joël Ouaknine, Karen Yorav, Edmund M. Clarke: Electr. Notes Theor. Comput. Sci. 89(3): 417-432 (2003)

Abstraction and counterexample-guided refinement in model checking of hybrid systems. Edmund M. Clarke, Ansgar Fehnker, Zhi Han, Bruce Krogh, Joel Ouaknine, Olaf Stursberg, and Michael Theobald: International Journal of Foundations of Computer Science 14(4), 2003.

Counterexample-guided abstraction refinement for symbolic model checking. Edmund M. Clarke, Orna Grumberg, Somesh Jha, Yuan Lu, and Helmut Veith: JACM 50(5): 752-794 (2003).

Verification of Out-of-Order Processor Designs Using Model Checking and Light-Weight Completion Function, Edmund M. Clarke, Sergey Berezin, Armin Biere, and Yunshan Zhu, FORMAL METHODS IN SYSTEM DESIGN, Vol. 20, No. 2, pp. 152-186, 2002.

Program slicing for VHDL. Edmund M. Clarke, Masahiro Fujita, Sreeranga P. Rajan, Thomas W. Reps, Subash Shankar, Tim Teitelbaum: STTT 4(1): 125-137 (2002)

State Space Reduction Using Partial Order Techniques. E. M. Clarke, M. Minea, O. Grumberg and D. Peled, SOFTWARE TOOLS FOR TECHNOLOGY TRANSFER, Vol. 3, No. 1, 1999, pp. 279-287.

Bounded Model Checking Using Satisfiability Solving. Edmund M. Clarke, Armin Biere, Richard Raimi, Yunshan Zhu: Formal Methods in System Design 19(1): 7-34 (2001).

The Verus language: representing time efficiently with BDDs. Edmund M. Clarke, Sérgio Vale and Aguiar Campos, Theor. Comput. Sci. 253(1): 95-118 (2001) 2000.

Program Slicing for {VHDL}. E. M. Clarke, M. Fujita, P.S. Rajan, T. Reps, S. Shankar and T. Teitelbaum. SOFTWARE TOOLS FOR TECHNOLOGY TRANSFER , Volume 4, Number 1, October 2002. p 125-137. Appeared online on October 9, 2001.

Selective Quantitative Analysis and Interval Model Checking: Verifying Different Facets of a System. E. M. Clarke, S. Campos, O. Grumberg, FORMAL METHODS IN SYSTEM DESIGN, Volume 17, Number 2, October 2000.

NuSMV: A New Symbolic Model Checker. E. M. Clarke, A. Cimatti, F. Giumchiglia and M. Roveri. SOFTWARE TOOLS FOR TECHNOLOGY TRANSFER, vol. 2 (4), p. 410, 2000.

Verification of a safety-critical railway interlocking system with real-time constraints. Edmund M. Clarke, Vicky Hartonas-Garmhausen, Sergio Campos, Alessandro Cimatti, and Fausto Giunchiglia Elsevier, SCIENCE JOURNAL SCIENCE OF COMPUTER PROGRAMMING, 36 (1) pp. 53-64 2000.

Automatic verification of hardware and software systems. Edmund M. Clarke: ACM SIGSOFT Software Engineering Notes 25(1): 41-42 (2000)

Verifying security protocols. Edmund M. Clarke, Somesh Jha, Wilfredo R. Marrero: with Brutus. ACM Trans. Softw. Eng. Methodol. 9(4): 443-487 (2000)

On the Semantic Foundations of Probabilistic Synchronous Reactive Programs. Christel Baier, Edmund M. Clarke, Vasilili Hartonas-Garmhausen: Electr. Notes Theor. Comput. Sci. 22: 3-28 (1999)

Combining Local and Global Model Checking. Armin Biere, Edmund M. Clarke, Yunshan Zhu: Electr. Notes Theor. Comput. Sci. 23(2): 34-45 (1999)

Model Checking Semi-Continuous Time Models Using BDDs. Sérgio Vale Aguiar Campos, Marcio Teixeira, Marius Minea, Andreas Kuehlmann, Edmund M. Clarke: Electr. Notes Theor. Comput. Sci. 23(2): 75-87 (1999)

Verifying the SRT Division Algorithm Using Theorem Proving Techniques. E. M. Clarke, S. German and X. Zhao, FORMAL METHODS IN SYSTEM DESIGN, vol. 14, no. 1, pp. 7-44, January 1999.

The Analysis and Verification of Real-Time Systems Using Quantitative Symbolic Algorithms. E. M. Clarke and S. Campos, *INTERNATIONAL JOURNAL ON SOFTWARE TOOLS FOR TECHNOLOGY TRANSFER,* vol. 2(3), p.260, 1999.

Analysis and Verification of Real-Time Systems Using Quantitative Symbolic Algorithms. Sérgio Vale Aguiar Campos, Edmund M. Clarke: STTT 2(3): 260-269 (1999)

State Space Reduction Using Partial Order Techniques. Edmund M. Clarke, Orna Grumberg, Marius Minea, Doron Peled: STTT 2(3): 279-287 (1999)

Analytica: An Experiment in Combining Theorem Proving and Symbolic Computation. E.Clarke, A. Bauer and X. Zhao, *JOURNAL OF AUTOMATED REASONING,* vol. 21, pp. 295, 1998.

Formal Methods in System Design. Edmund M. Clarke: Editorial. 10(1): 5 (1997)

Another Look at LTL Model Checking. Edmund M. Clarke, Orna Grumberg, Kiyoharu Hamaguchi: Formal Methods in System Design 10(1): 47-71 (1997)

Verifying Parameterized Networks. E. M. Clarke O. Grumberg and S. Jha, ACM-TOPLAS, Vol. 19, No. 5, pp. 726-750, September 1997.

An Improved Algorithm for Evaluation of Fixpoint Expressions. E. M. Clarke, A. Browne, S. Jha, D. Long, and W. Marrero, *THEORETICAL COMPUTER SCIENCE,* Vol. 178, pp.237-255, 1997.

Symbolic Techniques for Formally Verifying Industrial Systems. E. M. Clarke, S. Campos and M. Minea, SCIENCE OF COMPUTER PROGRAMMING, Vol. 29, No. 1-2, pp. 79-98, July 1997.

Another Look at LTL Model Checking. E.Clarke, O. Grumberg and H. Hamaguchi, *FORMAL METHODS IN SYSTEM DESIGN, vol. 10, no. 1, pp. 47-71, February* 1997.

Spectral Transforms for Large Boolean Functions with Applications to Technology Mapping. E. M. Clarke, K. Mcmillan, X. Zhao, M. Fujita and J. Yang, *FORMAL METHODS IN SYSTEM DESIGN, vol. 10, no. 2/3, pp. 137-148, April/May* 1997.

Tools and Partial Analysis. Edmund M. Clarke, Jeannette M. Wing: ACM Comput. Surv. 28(4es): 116 (1996)

Formal Methods: State of the Art and Future Directions. Edmund M. Clarke, Jeannette M. Wing: ACM Comput. Surv. 28(4): 626-643 (1996)

Exploiting Symmetry in Temporal Logic Model Checking. E. M. Clarke, R. Enders, T. Filkorn and S. Jha, *FORMAL METHODS IN SYSTEM DESIGN*, vol. 9, no.1/2., pp. 77-104, August 1996.

Computer-aided Verification. E. M. Clarke, R. Kurshan, *IEEE Spectrum*, Vol. 33, pp. 61-67, 1996.

Temporal Verification of Real-Time Systems. E. M. Clarke, S. Campos, W. Marrero, M. Minea, and H. Hiraishi, *IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS*, vol E78-D, no. 7, pp. 796-802, July 1995.

Verification of the Futurebus+ Cache Coherence Protocol. E. M. Clarke, O. Grumberg, H. Hiraishi, S. Jha, D. Long, K. McMillan, and L. Ness, *FORMAL METHODS IN SYSTEM DESIGN*, vol. 6, no. 2, pp. 217-232, March 1995.

Model Checking and Abstraction. E. M. Clarke, O. Grumberg and D. Long, *ACM-TOPLAS*, Vol. 16, No. 5, pp. 1512-1542, September 1994.

Symbolic Model Checking for Sequential Circuit Verification. E. M. Clarke, J. Burch, D. Long, K. McMillan, and D. Dill, *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTERGRATED CIRCUITS AND SYSTEMS*, Vol. 13, No. 4, pp. 401-424, April 1994.

New and used temporal models: Frank D. Anger, Edmund M. Clarke: An issue of time. Appl. Intell. 3(1): 5-15 (1993)

A Unified Approach for Showing Language Containment And Equivalence between Various Types of Ω-Automata, Edmund M. Clarke, Ioana A. Draghicescu and Robert P. Kurshan*, INFORMATION PROCESSING LETTERS*, Vol. 46, pp. 301-308, 1993.

Application of BDDs to CAD for Digital Systems, Edmund M. Clarke and Masahiro Fujita*, JOURNAL OF THE INFORMATION PROCESSING SOCIETY OF JAPAN*, Vol. 34, No. 5, pp. 609-616, May 1993.

Analytica: A Theorem Prover for Mathematica, E. M. Clarke and X. Zhao*, THE MATHEMATICA JOURNAL*, Vol. 3, No. 1, , pp. 56-71, Winter 1993.

A Synthesis of Two Approaches for Verifying Finite State Concurrent Systems, E. M. Clarke, O. Grumberg and R.P. Kurshan*, JOURNAL OF LOGIC AND COMPUTATION*, Vol. 2, No. 5, October 1992, pp. 605-618.

PARTHENON: A Parallel Theorem Prover for Non-Horn Clauses, Edmund M. Clarke, Soumitra Bose, David E. Long, and Spiro Michaylov*, JOURNAL OF AUTOMATED REASONING*, Vol. 8, August 1992, pp. 153-181.

Symbolic Model Checking: 10^{20} States and Beyond, with Jerry R. Burch, Kenneth L. McMillan, David L. Dill, and L.J. Hwang*, INFORMATION AND COMPUTATION* (Special Issue for the best papers from LICS'90), Vol. 98, No. 2, June 1992, pp. 142-170.

Automatic Verification of Sequential Control Systems using Temporal Logic, Edmund M. Clarke, Il Moon, Gary J. Powers, and Jerry R. Burch*, AMERICAN INSTITUTE OF CHEMICAL ENGINEERS JOURNAL*, Vol. 38, No. 1, January 1992, pp. 67-75.

Reasoning about Networks with Many Identical Finite State Processes. Michael C. Browne, Edmund M. Clarke, Orna Grumberg: Inf. Comput. 81(1): 13-31 (1989)

Reasoning about Procedures as Parameters in the Language L4, Edmund M. Clarke, Steve M. German and Joseph Y. Halpern*, INFORMATION AND COMPUTATION*, Vol. 83, No. 3, December 1989, pp. 265-359.

Reasoning about Networks with Many Identical Processes, E. M. Clarke, M. Browne and O. Grumberg*, INFORMATION AND COMPUTATION*, Vol. 81, No. 1, April 1989, pp. 13-31.

Characterizing Finite Kripke Structures in Propositional Temporal Logic. E. M. Clarke, M.C. Browne and O. Grumberg*, THEORETICAL COMPUTER SCIENCE*, Vol. 59, 1988, pp. 115-131.

Escher-A Geometrical Layout System for Recursively Defined Circuits. Edmund M. Clarke with Yulin Feng, *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*, Vol. 7, No. 8, August 1988, pp. 908-919.

Characterizing Finite Kripke Structures in Propositional Temporal Logic. Michael C. Browne, Edmund M. Clarke, Orna Grumberg: Theor. Comput. Sci. 59: 115-131 (1988)

Compiling Path Expressions into VLSI Circuits. E. M. Clarke, T.S. Anantharaman, M.J. Foster, and B. Mishra, *DISTRIBUTED COMPUTING*, Vol. 1, No. 3, 1986, pp. 150-166.

Distributed Computing Issues in Hardware Design. Edmund M. Clarke: Distributed Computing 1(4): 185-186 (1986)

Verification of Sequential Circuits Using Temporal Logic. Michael C. Browne, Edmund M. Clarke, David L. Dill, Bud Mishra: Automatic IEEE Trans. Computers 35(12): 1035-1044 (1986)

Automatic Verification of Finite-State Concurrent Systems Using Temporal Logic Specifications. Edmund M. Clarke, E. Allen Emerson, A. Prasad Sistla: ACM Trans. Program. Lang. Syst. 8(2): 244-263 (1986)

Automatic Verification of Sequential Circuits Using Temporal Logic, E. M. Clarke, M.C. Browne, D.L. Dill and B. Mishra, *IEEE TRANSACTIONS ON COMPUTERS*, Vol. C-35, No. 12, December 1986, pp. 1035-1044.

Automatic Verification of Asynchronous Circuits Using Temporal Logic. E.M. Clarke and D.L. Dill*, IEEE PROCEEDINGS*, Vol. 133, Pt. E, No. 5, September 1986, pp. 276-282.

Automatic Verification of Finite-State Concurrent Systems Using Temporal Logic Specifications. E.M. Clarke, E.A. Emerson and A.P. Sistla*, ACM TRANSACTIONS ON PROGRAMMING LANGUAGES AND SYSTEMS*, Vol. 8, No. 2, April 1986, pp. 244-263.

Hierarchical Verification of Asynchronous Circuits Using Temporal Logic, E.M. Clarke and B. Mishra, *THEORETICAL COMPUTER SCIENCE*, Vol. 38, 1985, pp. 269-291.

The Complexity of Propositional Linear Temporal Logic, E.M. Clarke and A.P. Sistla*, JOURNAL OF THE ASSOCIATION FOR COMPUTING MACHINERY*, Vol. 32, No. 3, July 1985, pp. 733-749.

Can Message Buffers be Axiomatized in Linear Temporal Logic?. E.M. Clarke, A.P. Sistla, N. Francez, and A. Meyer, *INFORMATION AND CONTROL*, Vol. 63, No. 1/2, October/November 1984, pp. 88-112.

Effective Axiomatizations of Hoare Logics, Edmund M. Clarke, Steven M. German and Joseph Y. Halpern, *JOURNAL OF THE ASSOCIATION FOR COMPUTING MACHINERY*, Vol. 30, No. 3, July 1983, pp. 612-636.

Using Branching Time Temporal Logic to Synthesize Synchronization skeletons, E. M. Clarke and E. Allen Emerson, *SCIENCE OF COMPUTING 2*, 1982, pp. 241-266.

Distributed Reconfiguration Strategies for Fault Tolerant Multiprocessor Systems, E.M. Clarke and C.N. Nikolaou, special issue on fault tolerant computing, *IEEE TRANSACTIONS ON COMPUTERS*, Vol. C-31, No. 8, August l982.

Task Management in Ada-A Critical Evaluation for Real-time Multiprocessors. Eric S. Roberts, Arthur Evans Jr., C. Robert Morgan, Edmund M. Clarke: Softw., Pract. Exper. 11(10): 1019-1051 (1981)

Proving Correctness of Coroutines Without History Variables. Edmund M. Clarke: Acta Inf. 13: 169-188 (1980)

Synthesis of Resource Invariants for Concurrent Programs. Edmund M. Clarke: ACM Trans. Program. Lang. Syst. 2(3): 338-358 (1980)

A Critical Evaluation of ADA for Multiprocessor Systems, E. M. Clarke, A. Evans, R. Morgan, and E. Roberts. *SOFTWARE: PRACTICE AND EXPERIENCE*, Vol. 11, 1981, pp. 1019-1051.

Proving Coroutines Without History Variables, *ACTA INFORMATICA*, Vol.13, 1980, pp. 169-188.

Synthesis of Resource Invariants, *TOPLAS*, Vol.2, No.3, July 1980, pp. 338-358.

Program Invariants as Fixed Points, *COMPUTING*, Vol. 2l, No.4, 1979, pp. 273-294.

Programming Language Constructs for Which it is Impossible to Obtain Good Hoare-like Axioms, *JOURNAL OF THE ASSOCIATION FOR COMPUTING MACHINERY*, Vol. 26, No.l, January 1979, pp. 129-147.

Papers Presented at Refereed Conferences and Workshops:

δ-Complete Decision Procedures for Satisfiability over the Reals. Sicun Gao, Jeremy Avigad, Edmund M. Clarke: IJCAR 2012: 286-300

Assume-Guarantee Abstraction Refinement for Probabilistic Systems: Anvesh Komuravelli, Corina S. Pasareanu, Edmund M. Clarke. CAV 2012: 310-326

Assumption Generation for Asynchronous Systems by Abstraction Refinement. Qiusong Yang, Edmund M. Clarke, Anvesh Komuravelli, Mingshu Li: FACS 2012: 260-276

Rare-event verification for stochastic hybrid systems. Paolo Zuliani, Christel Baier, Edmund M. Clarke: HSCC 2012: 217-226

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